1. (Original) An apparatus comprising:

a memory unit comprising a memory location to store a first data value;

a processing unit to generate an address value corresponding to the memory location;

a buffer unit to store at least a portion of the first data value and to provide at least a portion of the first data value to the processing unit in response to the address value being generated.

2. (Original) The apparatus of Claim 1, wherein at least a portion of the first data value

is to be provided to the processing unit from the buffer unit instead of at least a portion of the first data value stored in the memory unit.

3. (Original) The apparatus of Claim 1 further comprising buffer control logic to determine whether at least a portion of the first data value stored in the buffer unit corresponds to the address value.

4. (Original) The apparatus of Claim 3 wherein the buffer logic comprises overflow detection logic to detect whether the address value has been incremented or decremented.

5. (Original) The apparatus of Claim 3 wherein the buffer logic comprises an arithmetic

unit to increment or decrement the address value.

6. (Original) The apparatus of Claim 3 further comprising invalidation logic to invalidate

data stored in the buffer unit if a write operation is addressed to the memory location.

7. (Original) The apparatus of Claim 1 wherein the memory unit is a cache memory.

8. (Original) The apparatus of Claim 7 further comprising a plurality of buffer units to

store data stored within a plurality of locations within the cache memory.

9. (Original) A processor comprising:

a cache memory to store a plurality of data;

a processor core to generate addresses corresponding to data stored within the cache memory;

a plurality of buffers from which the processor core may retrieve copies of data stored within the cache memory, the plurality of buffers being associated with a plurality of locations within the cache memory.

10. (Original) The processor of Claim 9 further comprising a selection unit to select one

of the plurality of buffers from which to retrieve data.

11. (Original) The processor of Claim 10 further comprising alignment and signing logic

to appropriately shift and apply appropriate sign information to data stored within the buffer selected by the selection unit.

12. (Original) The processor of Claim 9 further comprising a buffer control unit to detect

whether an address generated by the processor core corresponds to data stored within any of the plurality of buffers, and if so, to select data within the plurality of buffers to which the address generated by the processor core corresponds.

13. (Original) The processor of Claim 12 further comprising validation indicators to indicate whether data stored within the load buffers is valid.

14. (Original) The processor of Claim 13 wherein the validation indicators are to indicate

that data within all of the load buffers is invalid if the processor core has performed or will perform a write operation to a location within the cache memory to which a load buffer corresponds.

15. (Original) The processor of Claim 13 wherein the validation indicators are to indicate

that data within a load buffer is invalid if the processor core has performed or will perform a write operation to a location within the cache memory to which the load buffer corresponds.

16. (Original) The processor of Claim 15 further comprising a plurality of tag storage units to store portions of the cache memory address to which the load buffers correspond.

17. (Original) The processor of Claim 16 further comprising a comparator unit to compare contents of the tag storage unit to a portion of a cache memory address generated by the processor core.

18. (Canceled) A system comprising:

a memory unit to store a load instruction;

a microprocessor to execute the load instruction and to decode information within the load instruction in order to retrieve load data addressed by the load instruction from a load buffer, the load buffer comprising a plurality of load buffer entries associated with a plurality of cache entries such that the load data may be retrieved from the plurality of buffer entries instead of from the cache entries.

19. (Canceled) The system of Claim 18 wherein the information to be decoded comprises

a load address to index locations within the cache.

20. (Canceled) The system of Claim 19 wherein the microprocessor comprises a load

buffer control unit to detect whether the load address corresponds to data stored within any of the plurality of load buffer entries, and if so, to select data within the plurality of load buffer entries to which the load address corresponds.

21. (Canceled) The system of Claim 20 further comprising validation indicators to indicate whether data stored within the load buffer entries is valid.

22. (Canceled) The system of Claim 21 wherein the validation indicators are to indicate

that data within all of the load buffer entries is invalid if the processor core has performed or will perform a write operation to a location within the cache to which a load buffer entry corresponds.

23. (Canceled) The system of Claim 22 wherein the validation indicators are to indicate

that data within a load buffer entry is invalid if the processor core has performed or will perform a write operation to a location within the cache memory to which the load buffer entry corresponds.

24. (Canceled) The system of Claim 23 wherein the execution of the load instruction is to

cause the load address to be modified by an incremental amount.

25. (Canceled) The system of Claim 23 wherein the execution of the load instruction is to

cause the load address to be modified according to an arithmetic operation.

26. (Canceled) The system of Claim 23 wherein the execution of the load instruction is to

cause the load address to be modified according to a register assignment.

27. (Canceled) A method comprising:

detecting a load address corresponding to a location within a cache;

determining whether the cache load address corresponds to load data stored within any of a plurality of load buffer entries;

retrieving the load data from one of the plurality of load buffer entries instead of from the cache if the cache load address corresponds to load data stored within any of the plurality of load buffer entries.

28. (Canceled) The method of Claim 27 wherein the determination of whether the cache

load address corresponds to load data stored within any of the plurality of load buffer entries comprises detecting whether the load address corresponds to a buffer entry address.

29. (Canceled) The method of Claim 28 wherein the detection of whether the load address corresponds to a buffer entry address comprises detecting an overflow bit in an address register storing the load address.

30. (Canceled) The method of Claim 28 wherein the detection of whether the load address corresponds to a buffer entry address comprises performing a mask operation to a register storing the load address.

31. (Canceled) The method of Claim 28 wherein the detection of whether the load address corresponds to a buffer entry address comprises performing an address compare operation between a portion of the load address and a buffer entry address.

32. (Canceled) The method of Claim 27 further comprising invalidating all of the plurality

of store buffer entries if a write operation occurs to a cache address corresponding to a buffer entry address.

33. (Canceled) The method of Claim 27 further comprising invalidating only one store

buffer entry if a write operation occurs to a cache address to which the store buffer entry corresponds.